



UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. |
|-----------------|-------------|----------------------|---------------------|
|-----------------|-------------|----------------------|---------------------|

09/144,579 08/31/98 TSANG

D 1138-71

MARGER JOHNSON & MCCOLLOM  
1030 S W MORRISON STREET  
PORTLAND OR 97205

MMC2/1121

EXAMINER

LOKE, S

ART UNIT

PAPER NUMBER

2811

DATE MAILED:

11/21/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

# Office Action Summary

Application No.  
**09/144,579**

Applicant(s)  
**Tsang et al.**

Examiner  
**Loke**

Group Art Unit  
**2811**



☒ Responsive to communication(s) filed on Sep 5, 2000

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

## Disposition of Claims

☒ Claim(s) 23 and 30-42 is/are pending in the application.

Of the above, claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

☐ Claim(s) \_\_\_\_\_ is/are allowed.

☒ Claim(s) 23 and 30-42 is/are rejected.

☐ Claim(s) \_\_\_\_\_ is/are objected to.

☐ Claims \_\_\_\_\_ are subject to restriction or election requirement.

## Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on \_\_\_\_\_ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some\* ☐ None of the CERTIFIED copies of the priority documents have been  
☐ received.

☐ received in Application No. (Series Code/Serial Number) \_\_\_\_\_.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\*Certified copies not received: \_\_\_\_\_

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

## Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). \_\_\_\_\_

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

Art Unit: 2811

1. Claims 33 and 38 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Fig. 14 discloses the first trench has a predetermined depth [156A] within the N+ substrate [122] (second layer). The specification never discloses the first trench has a predetermined depth within the first layer as claimed in claim 33.

The specification discloses the second embodiment (fig. 20) having a sidewall spacer with a lateral thickness of 0.8 to 1.0 microns (page 16, lines 19-21). The specification never discloses the lateral thickness of the vertically-oriented insulative layer of the second embodiment is in a range of 0.5 to 1.0 microns as claimed in claim 38.

2. Claims 23 and 30-38 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 34, line 34, "the trench sidewalls" is unclear whether it is being referred to "the second trench sidewalls".

In claim 36, line 2, "said vertically-oriented layers" has no antecedent basis.

In claim 31, line 2, "said first trenches", and lines 2-3, "said vertically oriented layers" have no antecedent basis.

Art Unit: 2811

In claim 31, line 4, it is unclear whether each of the first trenches containing the gate oxide layer and gate conductor.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 23, 31, 32, and 34-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Davies.

Sakamoto discloses a transistor in figs. 4(d) and 5(d). It comprises: a gate trench [8] formed on a drain substrate [1,3]; p-type body region [11] and vertical channel and source regions [11, 12] formed between the trenches; insulating layer [4, 9, 9'] formed adjacent to the gate electrode [8]; source electrode [15] formed on the regions [11, 12, 9, 9'].

Sakamoto differs from the claimed invention by not showing a p<sup>+</sup> type body region.

Davies shows a p<sup>+</sup> type body region [21] formed in a p-type base region [17] in a vertical MOSFET in fig. 1.

Since both Sakamoto and Davies teach a vertical MOSFET, it would have been obvious to have the p<sup>+</sup> type body region of Davies in Sakamoto because it prevents parasitic bipolar transistor turn on and it extends the safe operating area of the transistor.

Art Unit: 2811

In regards to claim 34, it would have been obvious for the vertically-oriented layer having a lateral thickness of less than 0.5  $\mu\text{m}$  because it depends on the size of the transistor cell and the packing density of the transistor cells.

In regards to claim 23, it would have been obvious for the first vertical layer portion has a lateral thickness less than one micron because it depends on the size of the transistor cell and the packing density of the transistor cells.

In regards to claim 32, figs. 4(d) and 5(d) of Sakamoto differs from the claimed invention by not showing a base region made of p-type layer.

Fig. 7 of Sakamoto shows a p-type layer [1'] formed under the n-type layer [2, 3].

Since figs. 4(d), 5(d) and 7 of Sakamoto show a vertical transistor, it would have been obvious to have the p-type layer of fig. 7 in figs. 4(d) and 5(d) of Sakamoto because it can form a pnpn type transistor.

5. Claims 30 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Davies, further in view Blanchard.

In regards to claim 30, Sakamoto differs from the claimed invention by not showing each of the plurality of cells surrounded by the gate trench.

Blanchard shows each of the plurality of cells surrounded by the gate trench in fig. 9a.

Since both Sakamoto and Blanchard teach a vertical MOSFET with a trench gate, it would have been obvious to have the transistor cell structure of Blanchard in Sakamoto because it is a widely used transistor cell structure in power MOSFET.

Art Unit: 2811

In regards to claim 33, Sakamoto further differs from the claimed invention by not showing a trench gate oxide with two different thickness.

Blanchard shows the gate oxide layer [32] having a thick oxide layer at the bottom of the gate trench and a thin oxide layer at the upper portion of the gate trench in fig. 3.

Since both Sakamoto and Blanchard teach a vertical MOSFET with a trench gate, it would have been obvious to have the gate oxide layer of Blanchard in Sakamoto because it increases the breakdown voltage of the device.

6. Claims 37 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Davies, further in view of Wickstrom.

In regards to claim 37, Sakamoto differs from the claimed invention by not showing the insulating layer offset from a surface of the gate oxide.

Wickstrom shows an insulating layer [19] extends beyond the gate insulating layer [32] in fig. 19.

Since both Sakamoto and Wickstrom show a vertical transistor, it would have been obvious to have the insulating layer of Wickstrom in Sakamoto because it further improves the insulation between the gate electrode and the source electrode.

In regards to claim 38, it would have been obvious for the lateral thickness of the vertically-oriented insulative layer is in a range of 0.5 to 1.0 microns because it depends on the size of the cell and the packing density of the transistor cells.

Art Unit: 2811

7. Claims 39, 40 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto.

Sakamoto discloses a transistor in figs. 4(d) and 5(d). It comprises: a gate trench [8] formed on a drain substrate [1,3]; p-type body region [11] and vertical channel and source regions [11, 12] formed between the trenches; insulating layer [4, 9, 9'] formed adjacent to the gate electrode [8]; the vertically-insulative layers [4] being formed by a deposited film of uniform lateral thickness and the laterally-extending insulative layer [9, 9'] being separately formed of a deposited isolation material; source electrode [15] formed on the regions [11, 12, 9, 9'].

It would have been obvious to have the oxide material as the gate insulating layer because it is a widely used insulating material.

In regards to claim 39, it would have been obvious for the vertically-oriented layer having a lateral thickness of less than 0.5 um because it depends on the size of the transistor cell and the packing density of the transistor cells.

In regards to claim 42, it would have been obvious for the lateral thickness of the vertically-oriented insulative layer is in a range of 0.5 to 1.0 microns because it depends on the size of the transistor cell and the packing density of the transistor cells.

8. Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Wickstrom.

In regards to claim 41, Sakamoto differs from the claimed invention by not showing the insulating layer offset from a surface of the gate oxide.

Art Unit: 2811

Wickstrom shows an insulating layer [19] extends beyond the gate insulating layer [32] in fig. 19.

Since both Sakamoto and Wickstrom show a vertical transistor, it would have been obvious to have the insulating layer of Wickstrom in Sakamoto because it further improves the insulation between the gate electrode and the source electrode.

9. Applicant's arguments filed 9/5/00 have been fully considered but they are not persuasive.

It is urged, in pages 5-6 of the remarks, that page 10 of the specification discloses the thickness of the sidewall spacer is between 0.5 to 1.0 microns. However, claim 38 depends on claim 37 which is directed to the second embodiment of the invention (fig. 20). It is important to note that page 10 of the specification is directed to the first embodiment (figs. 12, 13). Since page 16 of the specification discloses the lateral thickness of the insulative layer of the second embodiment is in a range of 0.8 to 1.0 microns, the specification never discloses the claimed subject matter as claimed in claim 38.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920.

sl

November 20, 2000

Steven Loke  
Primary Examiner

